Code.No: RR310404 | RR | SET-1

III B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010
LINEAR IC APPLICATIONS
(ELECTRONICS AND COMMUNICATIONS ENGINEERING)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks

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1.a) Discuss the significance of the following Op-Amp AC characteristics
(i) Slew Rate (ii) CMRR (iii) SVRR (iv) Frequency compensation (External)
b) List the characteristics of 741 IC and compare these characteristics with that of an ideal operational amplifier. [8+8]

2.a) What is an I-to-V converter? Explain the I-V conversion process with the help of suitable circuit diagrams and relevant waveforms.
b) Draw the circuit diagram of an ideal Op-Amp integrator and derive an expression for its output voltage.
c) Explain how the deficiencies of an ideal integrator are overcome in a practical integrator. [6+5+5]

3.a) Draw the circuit diagram of a precision Full wave Rectifier and explain its operation with corresponding equivalent circuits individually for positive and negative half cycles of input signal.
b) Define Load and Line regulations of a Voltage regulator. Explain voltage regulation using shunt regulator based on 723 IC voltage regulator. [8+8]

4.a) Draw the block schematic of a 565, phase Locked Loop IC and explain the purpose of every block of it in capturing and locking to the frequency of incoming signal.
b) Describe how triangular waves can be generated using an Op-Amp square wave generator. [8+8]

5.a) Design a first order wideband Band pass filter by cascading a Low pass filter of cut-off frequency 20KHz and a 600Hz cut off high pass filter.
b) Draw the functional block diagram of a 555 time IC and list any four applications of 555 times IC. [8+8]

6.a) Define Lower & Upper trigger points of a Schmitt trigger comparator.
b) Derive an expression for the hysterises in an Op-Amp based Schmitt trigger comparator.
c) Define Lock and capture ranges of a phase Locked Loop. [6+5+5]

7.a) List the deficiencies of a weighted resistor type Digital-to-Analog converter and explain how these can be overcome in an inverted R-2R ladder type Digital-to-Analog converter.
b) If the resolution of a Digital-to-Analog converter is 10mV/LSB, determine the full scale output voltage and the output voltage for an input of
i) 1101 and ii) 10111101 [6+10]

8.a) Compare the performance characteristics of dual slope integration type, counter type, Flash type and successive application type Analog-to-Digital converters.
b) Describe the conversion process using a parallel comparator type Flash Analog-to-Digital converter circuit. [8+8]

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Code.No: RR310404 | RR | SET-2

III B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010
LINEAR IC APPLICATIONS
(ELECTRONICS AND COMMUNICATIONS ENGINEERING)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks

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1.a) Draw the circuit diagram of a precision Full wave Rectifier and explain its operation with corresponding equivalent circuits individually for positive and negative half cycles of input signal.
b) Define Load and Line regulations of a Voltage regulator. Explain voltage regulation using shunt regulator based on 723 IC voltage regulator. [8+8]

2.a) Draw the block schematic of a 565, phase Locked Loop IC and explain the purpose of every block of it in capturing and locking to the frequency of incoming signal.
b) Describe how triangular waves can be generated using an Op-Amp square wave generator. [8+8]

3.a) Design a first order wideband Band pass filter by cascading a Low pass filter of cut-off frequency 20KHz and a 600Hz cut off high pass filter.
b) Draw the functional block diagram of a 555 time IC and list any four applications of 555 times IC. [8+8]

4.a) Define Lower & Upper trigger points of a Schmitt trigger comparator.
b) Derive an expression for the hysterises in an Op-Amp based Schmitt trigger comparator.
c) Define Lock and capture ranges of a phase Locked Loop. [6+5+5]

5.a) List the deficiencies of a weighted resistor type Digital-to-Analog converter and explain how these can be overcome in an inverted R-2R ladder type Digital-to-Analog converter.
b) If the resolution of a Digital-to-Analog converter is 10mV/LSB, determine the full scale output voltage and the output voltage for an input of
i) 1101 and ii) 10111101 [6+10]

6.a) Compare the performance characteristics of dual slope integration type, counter type, Flash type and successive application type Analog-to-Digital converters.
b) Describe the conversion process using a parallel comparator type Flash Analog-to-Digital converter circuit. [8+8]

7.a) Discuss the significance of the following Op-Amp AC characteristics
(i) Slew Rate (ii) CMRR (iii) SVRR (iv) Frequency compensation (External)
b) List the characteristics of 741 IC and compare these characteristics with that of an ideal operational amplifier. [8+8]

8.a) What is an I-to-V converter? Explain the I-V conversion process with the help of suitable circuit diagrams and relevant waveforms.
b) Draw the circuit diagram of an ideal Op-Amp integrator and derive an expression for its output voltage.
c) Explain how the deficiencies of an ideal integrator are overcome in a practical integrator. [6+5+5]

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Code.No: RR310404 | RR | SET-3

III B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010
LINEAR IC APPLICATIONS
(ELECTRONICS AND COMMUNICATIONS ENGINEERING)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks

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1.a) Design a first order wideband Band pass filter by cascading a Low pass filter of cut-off frequency 20KHz and a 600Hz cut off high pass filter.
b) Draw the functional block diagram of a 555 time IC and list any four applications of 555 times IC. [8+8]

2.a) Define Lower & Upper trigger points of a Schmitt trigger comparator.
b) Derive an expression for the hysterises in an Op-Amp based Schmitt trigger comparator.
c) Define Lock and capture ranges of a phase Locked Loop. [6+5+5]

3.a) List the deficiencies of a weighted resistor type Digital-to-Analog converter and explain how these can be overcome in an inverted R-2R ladder type Digital-to-Analog converter.
b) If the resolution of a Digital-to-Analog converter is 10mV/LSB, determine the full scale output voltage and the output voltage for an input of
i) 1101 and ii) 10111101 [6+10]

4.a) Compare the performance characteristics of dual slope integration type, counter type, Flash type and successive application type Analog-to-Digital converters.
b) Describe the conversion process using a parallel comparator type Flash Analog-to-Digital converter circuit. [8+8]

5.a) Discuss the significance of the following Op-Amp AC characteristics
(i) Slew Rate (ii) CMRR (iii) SVRR (iv) Frequency compensation (External)
b) List the characteristics of 741 IC and compare these characteristics with that of an ideal operational amplifier. [8+8]

6.a) What is an I-to-V converter? Explain the I-V conversion process with the help of suitable circuit diagrams and relevant waveforms.
b) Draw the circuit diagram of an ideal Op-Amp integrator and derive an expression for its output voltage.
c) Explain how the deficiencies of an ideal integrator are overcome in a practical integrator. [6+5+5]

7.a) Draw the circuit diagram of a precision Full wave Rectifier and explain its operation with corresponding equivalent circuits individually for positive and negative half cycles of input signal.
b) Define Load and Line regulations of a Voltage regulator. Explain voltage regulation using shunt regulator based on 723 IC voltage regulator. [8+8]

8.a) Draw the block schematic of a 565, phase Locked Loop IC and explain the purpose of every block of it in capturing and locking to the frequency of incoming signal.
b) Describe how triangular waves can be generated using an Op-Amp square wave generator. [8+8]

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Code.No: RR310404 | RR | SET-4

III B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010
LINEAR IC APPLICATIONS
(ELECTRONICS AND COMMUNICATIONS ENGINEERING)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks

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1.a) List the deficiencies of a weighted resistor type Digital-to-Analog converter and explain how these can be overcome in an inverted R-2R ladder type Digital-to-Analog converter.
b) If the resolution of a Digital-to-Analog converter is 10mV/LSB, determine the full scale output voltage and the output voltage for an input of
i) 1101 and ii) 10111101 [6+10]

2.a) Compare the performance characteristics of dual slope integration type, counter type, Flash type and successive application type Analog-to-Digital converters.
b) Describe the conversion process using a parallel comparator type Flash Analog-to-Digital converter circuit. [8+8]

3.a) Discuss the significance of the following Op-Amp AC characteristics
(i) Slew Rate (ii) CMRR (iii) SVRR (iv) Frequency compensation (External)
b) List the characteristics of 741 IC and compare these characteristics with that of an ideal operational amplifier. [8+8]

4.a) What is an I-to-V converter? Explain the I-V conversion process with the help of suitable circuit diagrams and relevant waveforms.
b) Draw the circuit diagram of an ideal Op-Amp integrator and derive an expression for its output voltage.
c) Explain how the deficiencies of an ideal integrator are overcome in a practical integrator. [6+5+5]

5.a) Draw the circuit diagram of a precision Full wave Rectifier and explain its operation with corresponding equivalent circuits individually for positive and negative half cycles of input signal.
b) Define Load and Line regulations of a Voltage regulator. Explain voltage regulation using shunt regulator based on 723 IC voltage regulator. [8+8]

6.a) Draw the block schematic of a 565, phase Locked Loop IC and explain the purpose of every block of it in capturing and locking to the frequency of incoming signal.
b) Describe how triangular waves can be generated using an Op-Amp square wave generator. [8+8]

7.a) Design a first order wideband Band pass filter by cascading a Low pass filter of cut-off frequency 20KHz and a 600Hz cut off high pass filter.
b) Draw the functional block diagram of a 555 time IC and list any four applications of 555 times IC. [8+8]

8.a) Define Lower & Upper trigger points of a Schmitt trigger comparator.
b) Derive an expression for the hysterises in an Op-Amp based Schmitt trigger comparator.
c) Define Lock and capture ranges of a phase Locked Loop. [6+5+5]

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